Chapter 1. Microblaze and DDR3

Microblaze 을 사용한 임베디드 시스템을 구현할 경우 메모리 콘트롤러가 필요한 경우가 많이 있습니다.

DDR2, 3 메모리의 경우에는 동작속도가 너무 높다 보니 일반적으로 RTL 로 메모리 콘트롤러를 구현하지 않습니다.

이때 사용하는 툴이 MIG 라는 툴인데 MIG 는 메모리 콘트롤러가 매우 높은 동작 주파수에서도 제대로 동작할 수 있도록 메모리 콘트롤러를 만들어 줍니다.

임베디드 시스템 에서도 메모리 콘트롤러를 사용하게 되는데 이 문서에서는 MIG 에서 만든 것을 EDK 에서 사용하는 방법을 보여 줍니다.

1.1 Device & Memory type

주어진 스펙은 다음과 같습니다.

- **Device : XC7K325TFFG900**
- **DDR : K4B4G1646B-HCK0 (2 개)**
- **http://www.samsung.com/global/business/semiconductor/file/product/ds_k4b4g1646b_rev10-1.pdf**
- **요청 Bank : 16, 17, 18 Bank (16bit 만 쓸 경우, 16, 17)**

다음은 4Gb 에 대한 어드레스 핀 갯수, 컬럼 어드레스 핀, 뱅크 어드레스 핀 갯수가 몇개인지 보여 줍니다.

MIG 를 통해 메모리 콘트롤러를 만들 때 아래와 같은 정보가 필요 합니다.

BC switch on the fly	$A_{12}/\overline{BC}$	$A_{12}/\overline{BC}$	$A_{12}/\overline{BC}$
Page size *1	1 KB	1 KB	2 KB

4Gb

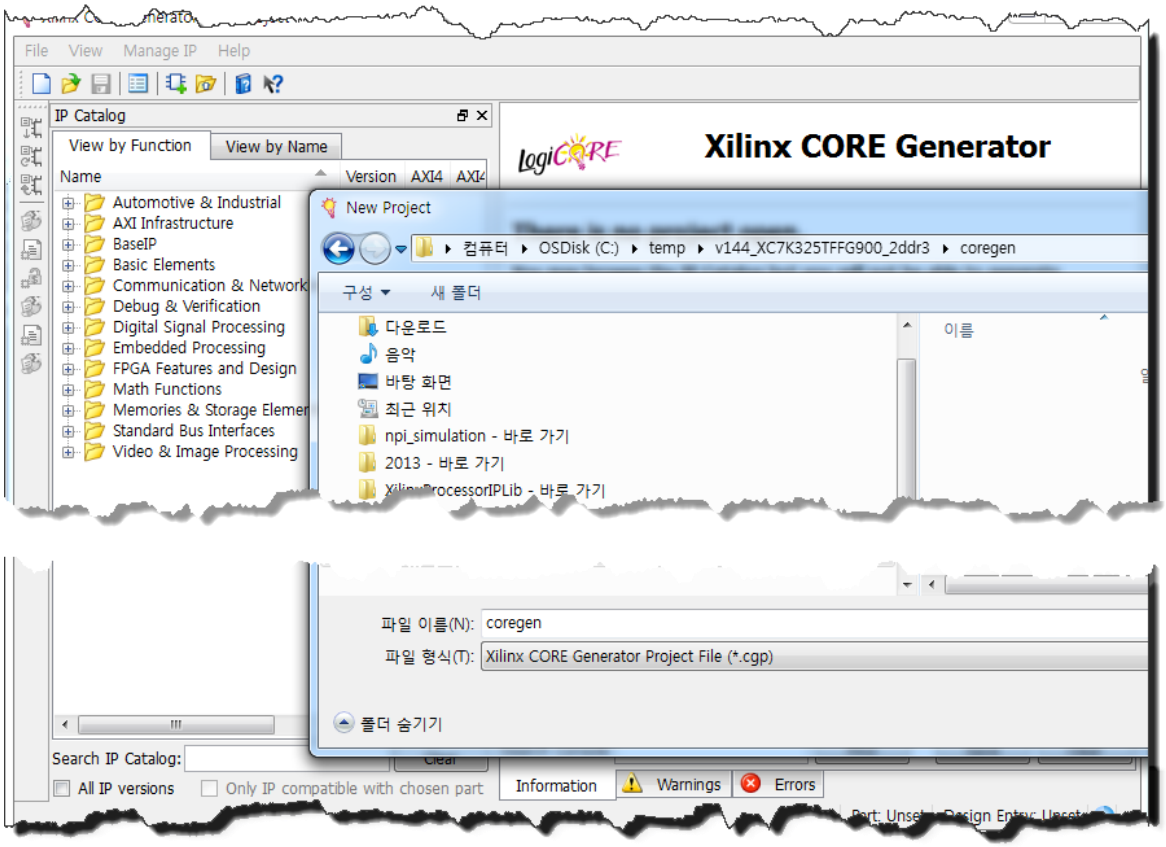
Configuration	1Gb x 4	512Mb x 8	256Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A_{10}/AP	A_{10}/AP	A_{10}/AP
Row Address	A_0 - A_{15}	A_0 - A_{15}	A_0 - A_{14}
Column Address	A_0 - A_9,A_{11}	A_0 - A_9	A_0 - A_9
BC switch on the fly	$A_{12}/\overline{BC}$	$A_{12}/\overline{BC}$	$A_{12}/\overline{BC}$
Page size *1	1 KB	1 KB	2 KB

8Gb

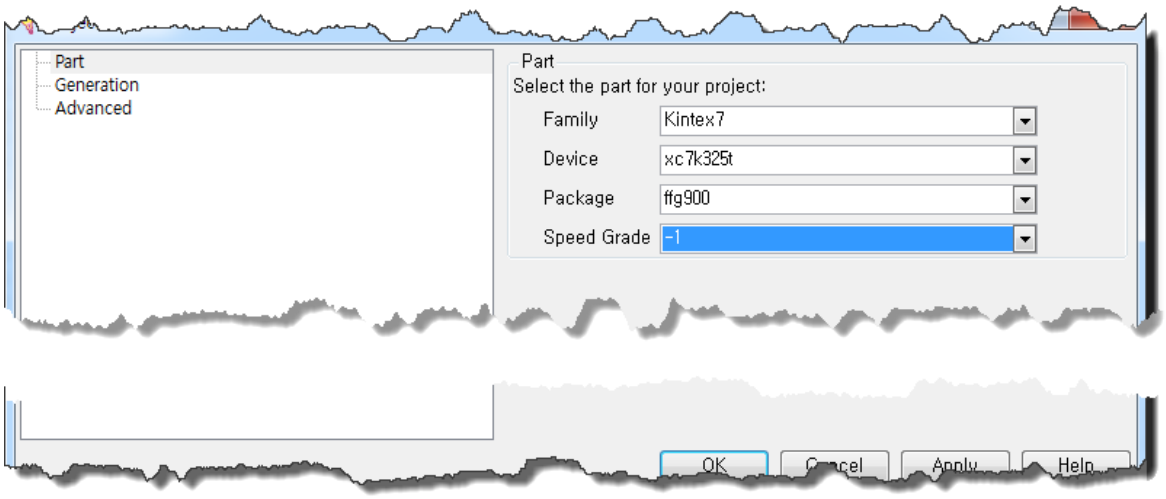
Configuration	2Gb x 4	1Gb x 8	512Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A_{10}/AP	A_{10}/AP	A_{10}/AP
Row Address	[illegible]	[illegible]	[illegible]

1.2 Coregen Design flow

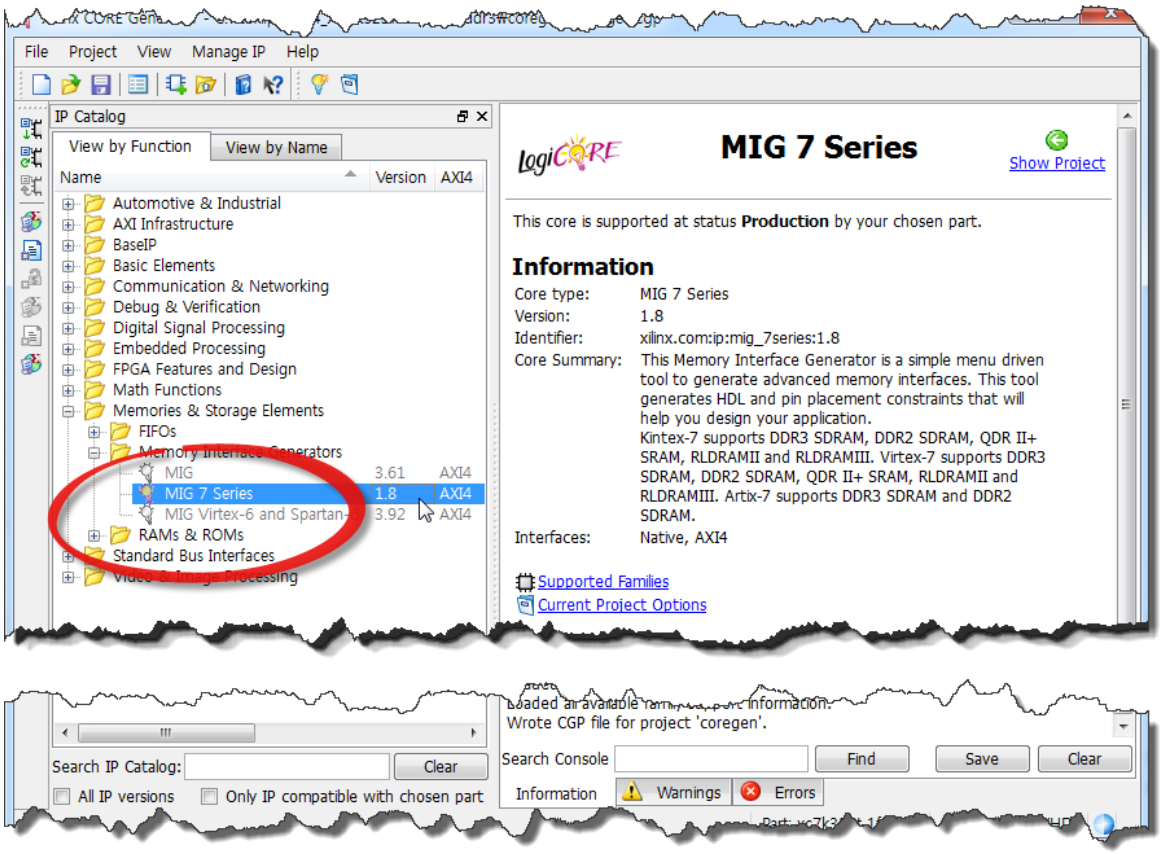
Coregen 에서 새로운 프로젝트를 등록 합니다.



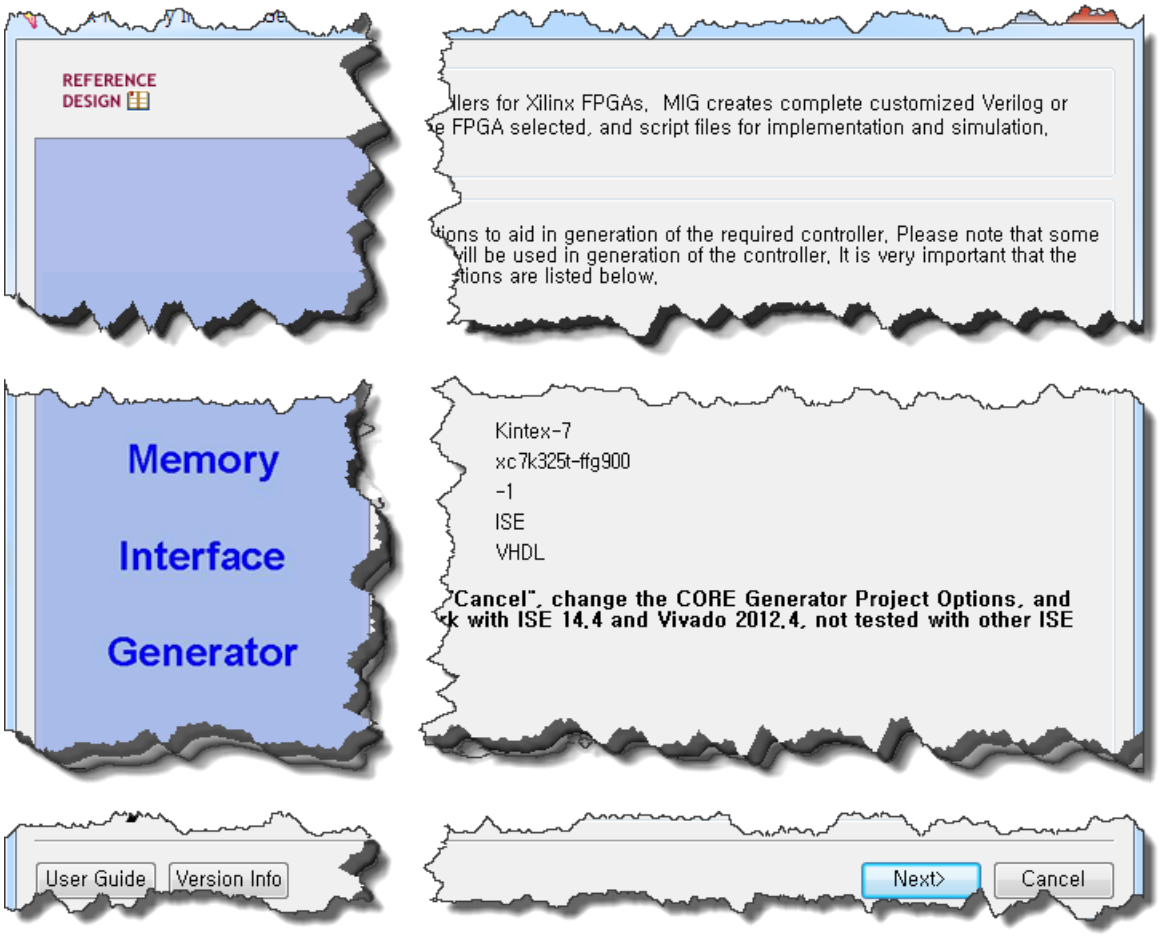
사용한 디바이스를 선택하고

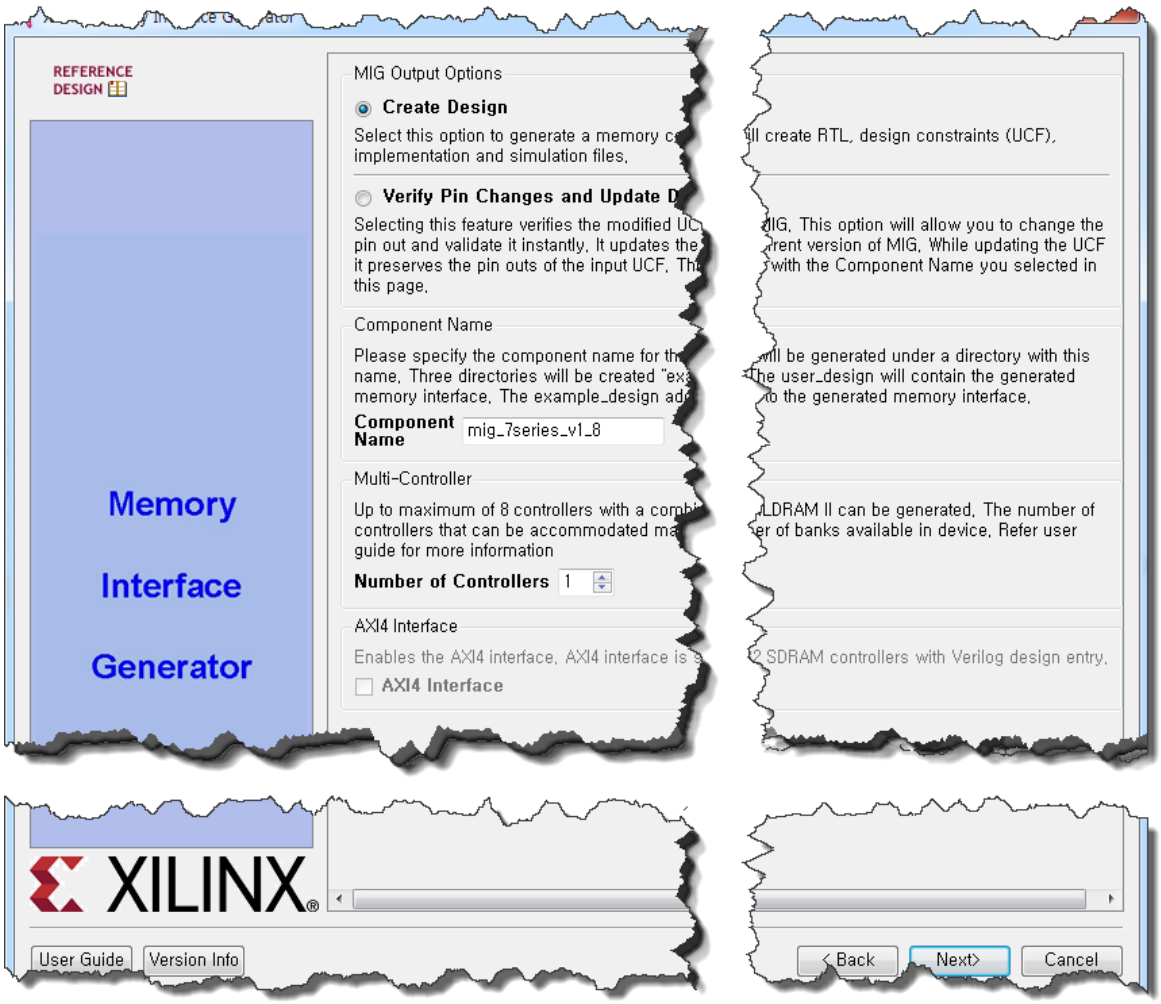


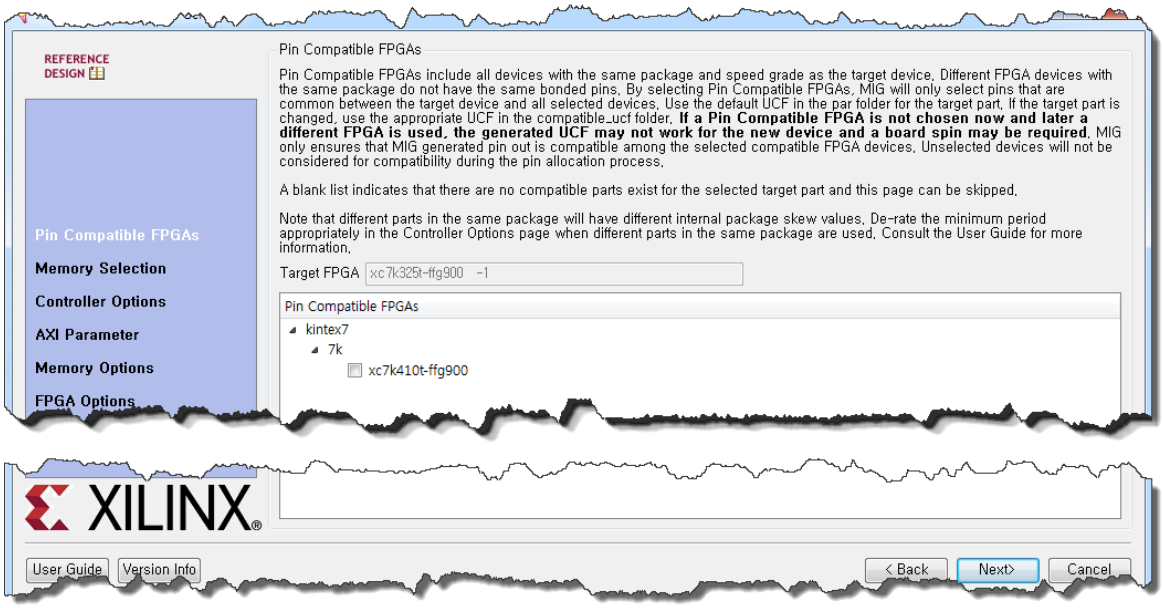
MIG 를 선택 합니다.

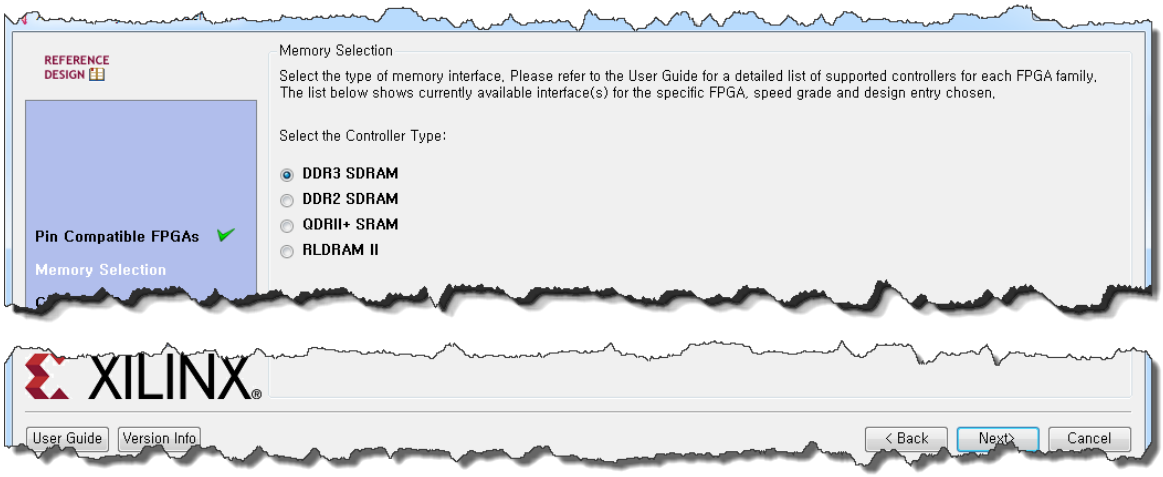


여기서 부터 별 얘기가 없으면 Defaul 나 Next 를 선택 합니다.

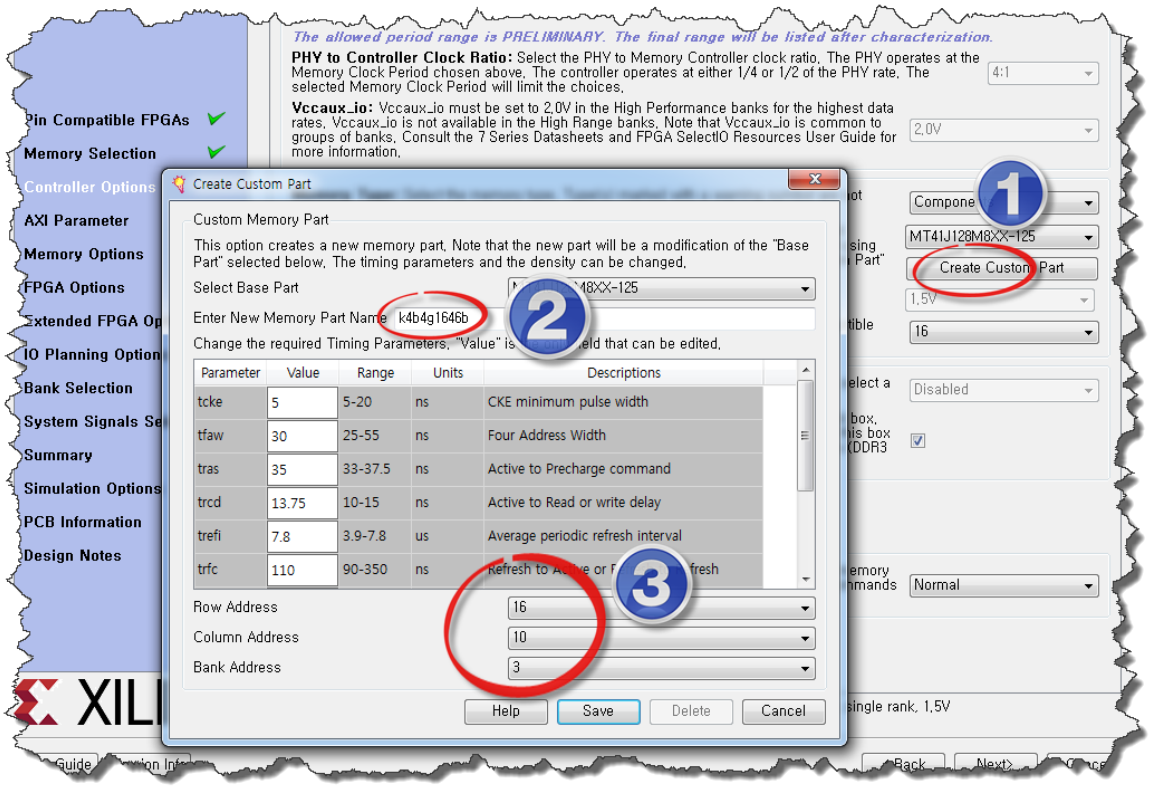

REFERENCE
DESIGN
llers for Xilinx FPGAs, MIG creates complete customized Verilog or
e FPGA selected, and script files for implementation and simulation.
ions to aid in generation of the required controller. Please note that some
vill be used in generation of the controller. It is very important that the
tions are listed below.
Memory
Interface
Generator
Kintex-7
xc7k325t-ffg900
-1
ISE
VHDL
"Cancel", change the CORE Generator Project Options, and
k with ISE 14.4 and Vivado 2012.4, not tested with other ISE
User Guide
Version Info
Next>
Cancel


REFERENCE DESIGN
Memory
Interface
Generator
MIG Output Options
Create Design
Verify Pin Changes and Update D
Component Name
Component Name
mig_7series_v1_8
Multi-Controller
Number of Controllers
1
AXI4 Interface
AXI4 Interface
XILINX
User Guide
Version Info
< Back
Next>
Cancel

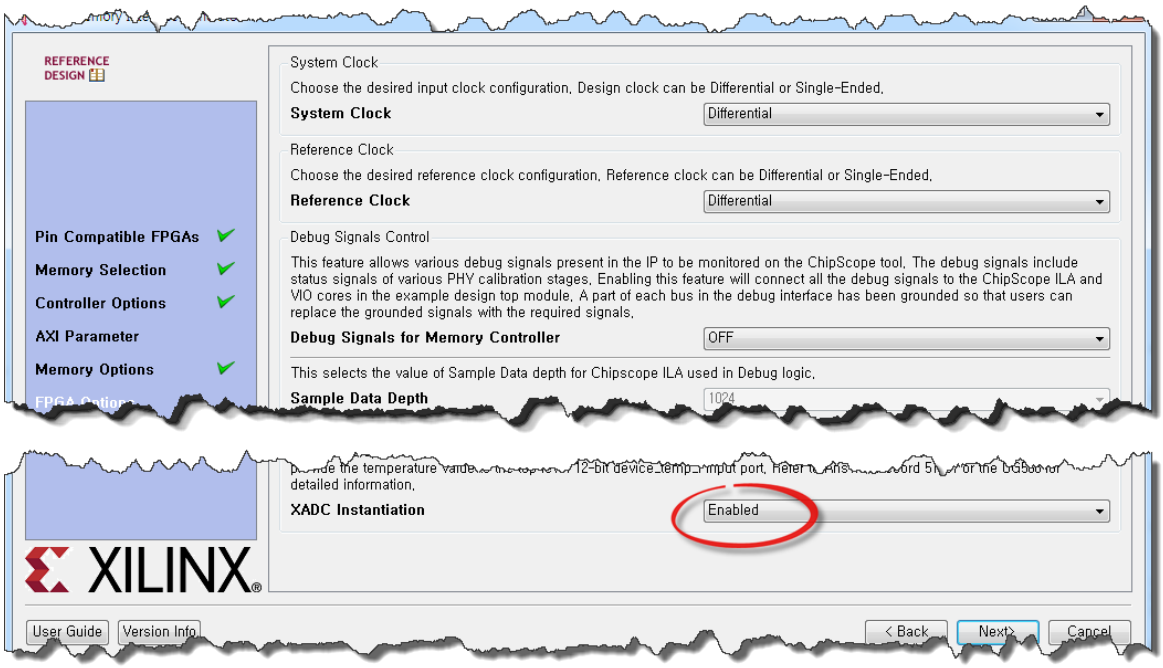

REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Pin Compatible FPGAs
Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default UCF in the par folder for the target part. If the target part is changed, use the appropriate UCF in the compatible_ucf folder. If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated UCF may not work for the new device and a board spin may be required. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.
A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.
Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.
Target FPGA
xc7k325t-ffg900 -1
Pin Compatible FPGAs
kintex7
7k
xc7k410t-ffg900
XILINX
User Guide
Version Info
< Back
Next>
Cancel

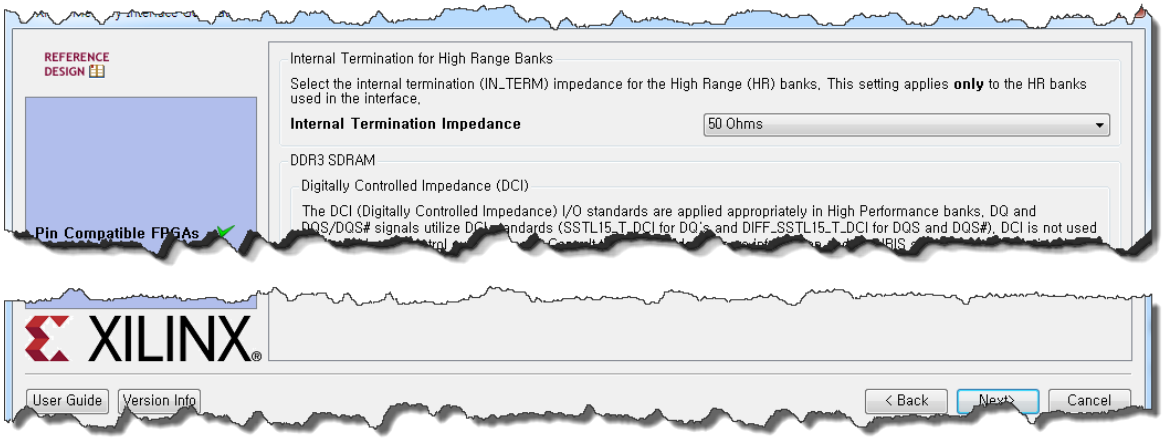


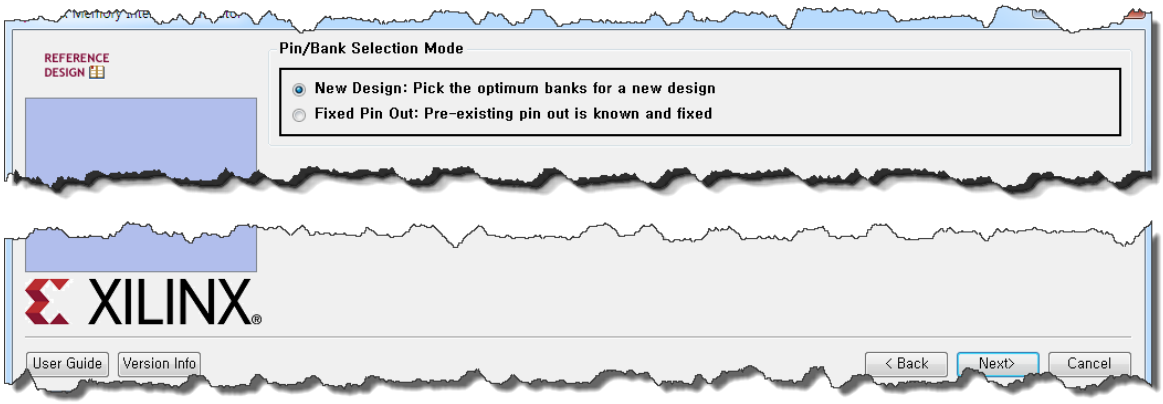
요기가 중요한 그림 입니다. 기본적으로 MIG 는 여러 메모리에 데이터베이스가 있는데 그중 하나를 선택할 수 있고 그렇지 않은 경우 아래 그림처럼 차례대로 선택 합니다. 3 번에서 어드레스 갯수, 컬럼 갯수, 뱅크 갯수를 데이터 쉬트처럼 선택 합니다. 나머지 타이밍은 데이터 쉬트를 참고해서 정해 줍니다.



대부분의 FPGA 에는 AD Convert 가 들어가 있는데 메모리 콘트롤러의 안정적인 동작을 위해 FPGA 의 온도를 읽어 타이밍을 보정하는데 사용하도록 합니다. 기본값은 'enable' 입니다.

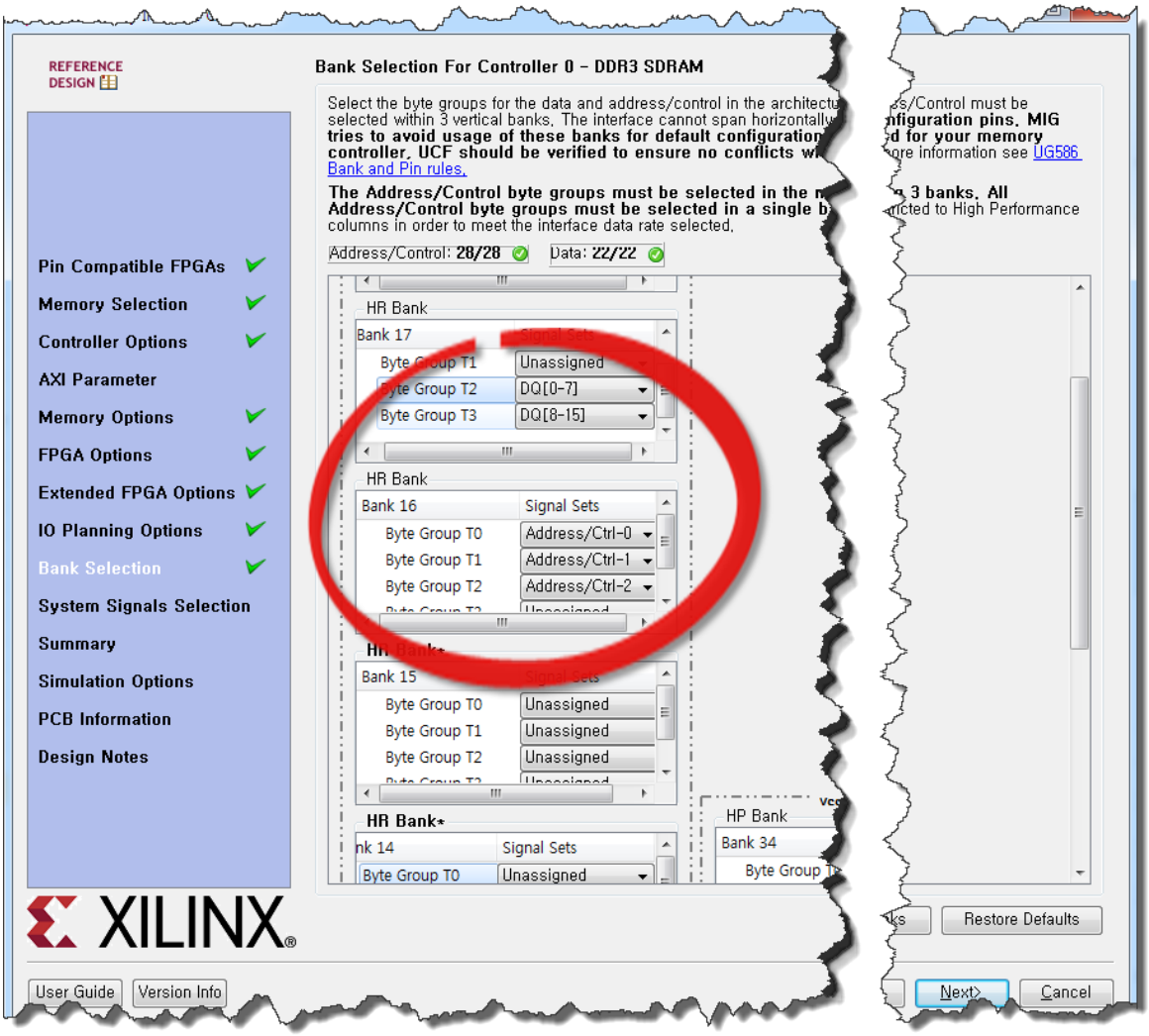




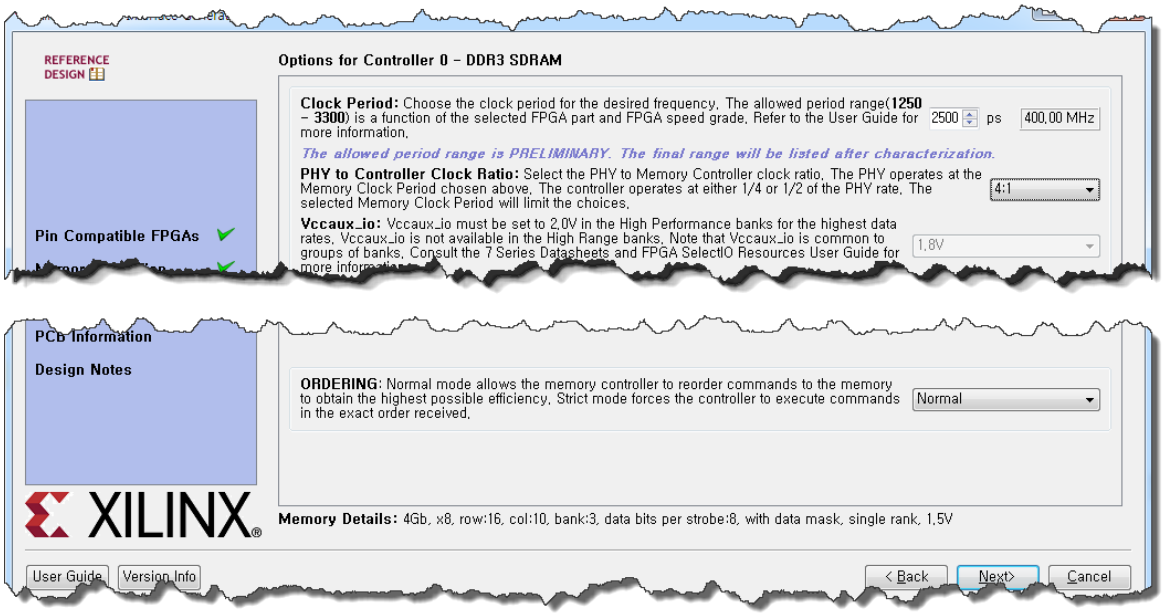


MIG 로 만든 메모리 콘트롤러는 기본적으로 최고 성능을 내도록 합니다. FPGA 에는 HR bank 와 HP bank 가 있는데 기본 뱅크는 HP 뱅크를 써야 합니다.

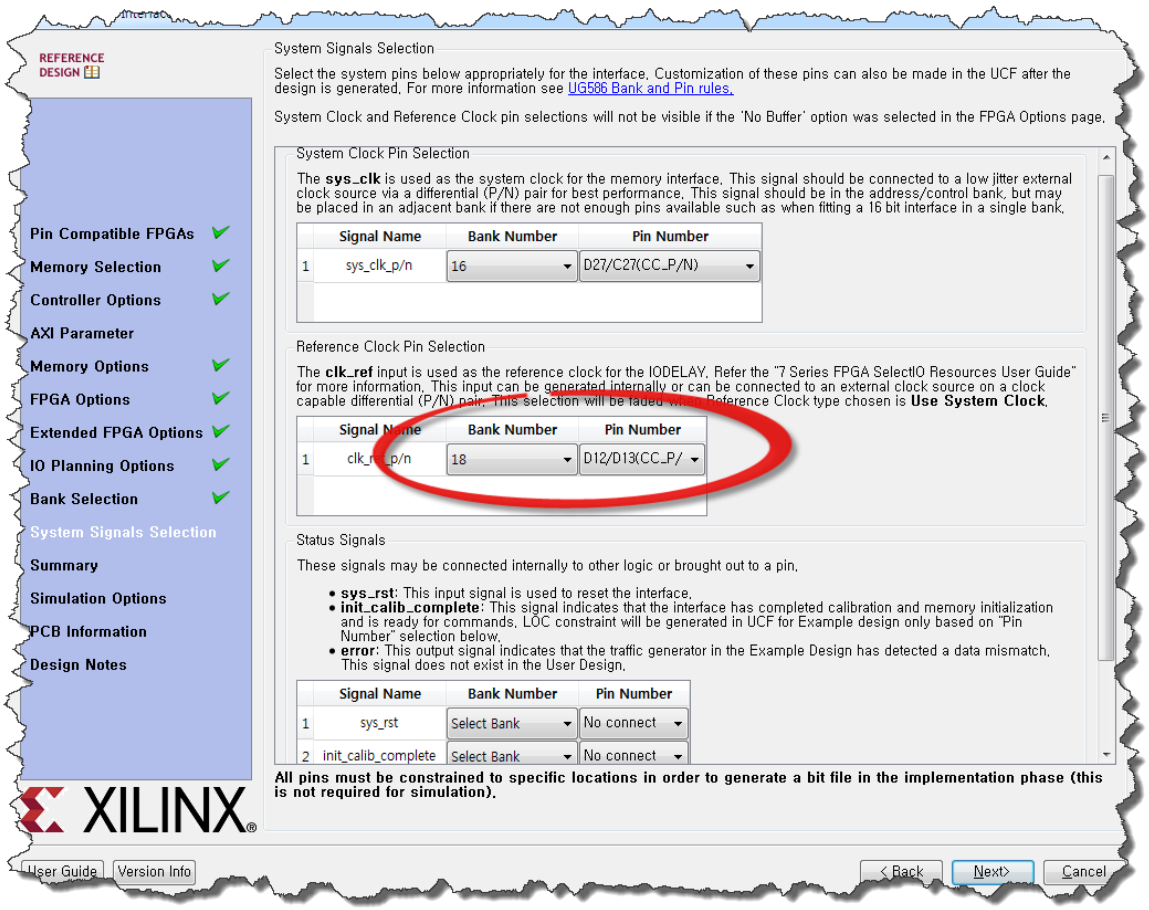
아래 그림과 같인 Bank16, Bank17 인 HR 뱅크를 사용하려면 메모리의 동작 주파수를 낮춰야 합니다.



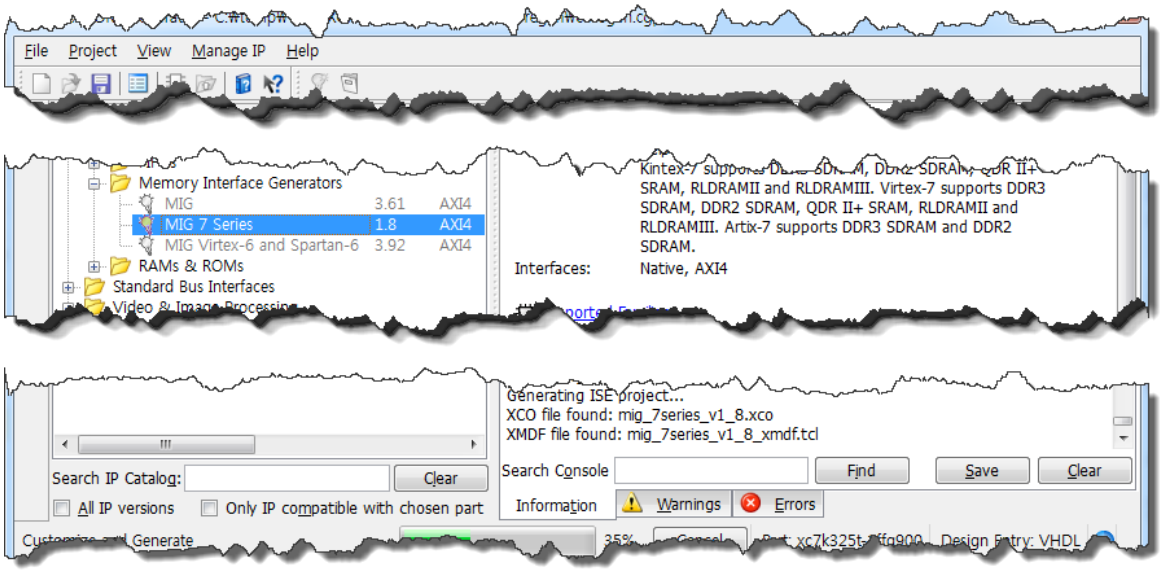
앞에 그림에서 잠시 스쳐 지나갔지만 MIG 는 기본 800Mhz 로 동작시키려고 합니다. 이 부분은 400Mhz 로 낮추었습니다.



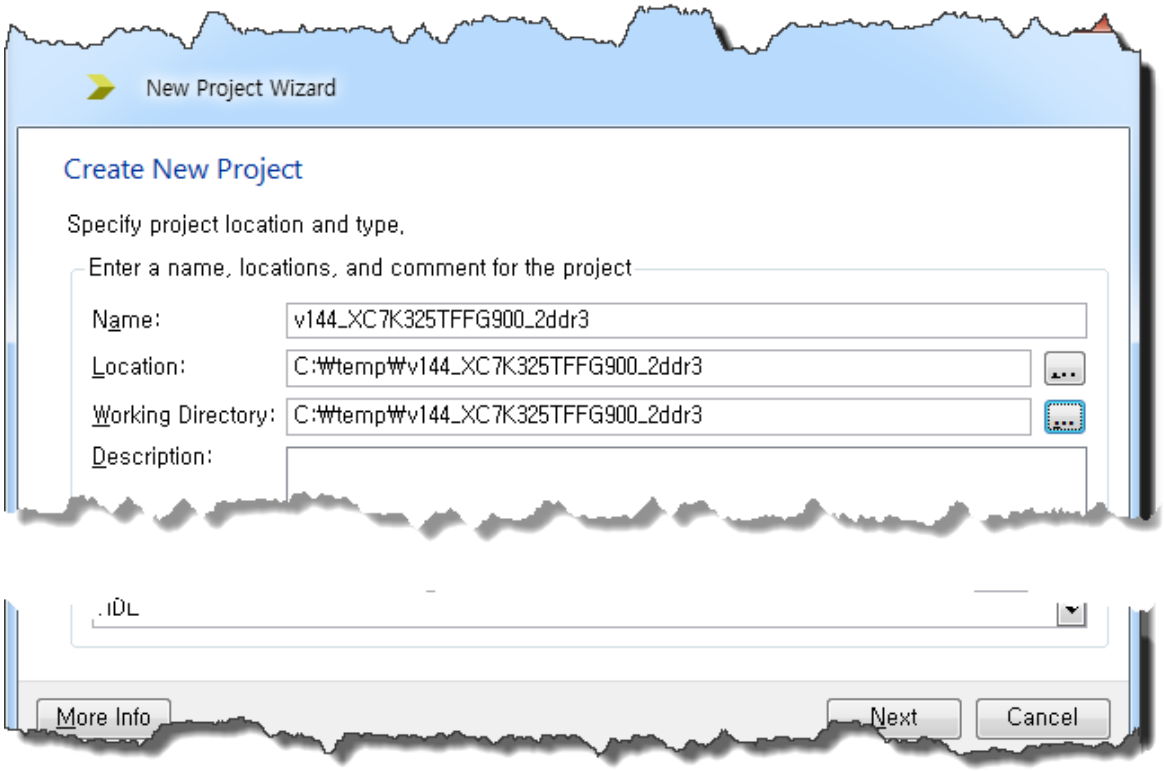
메모리 콘트롤러가 필요로 하는 클럭 정보를 넣어 줍니다.

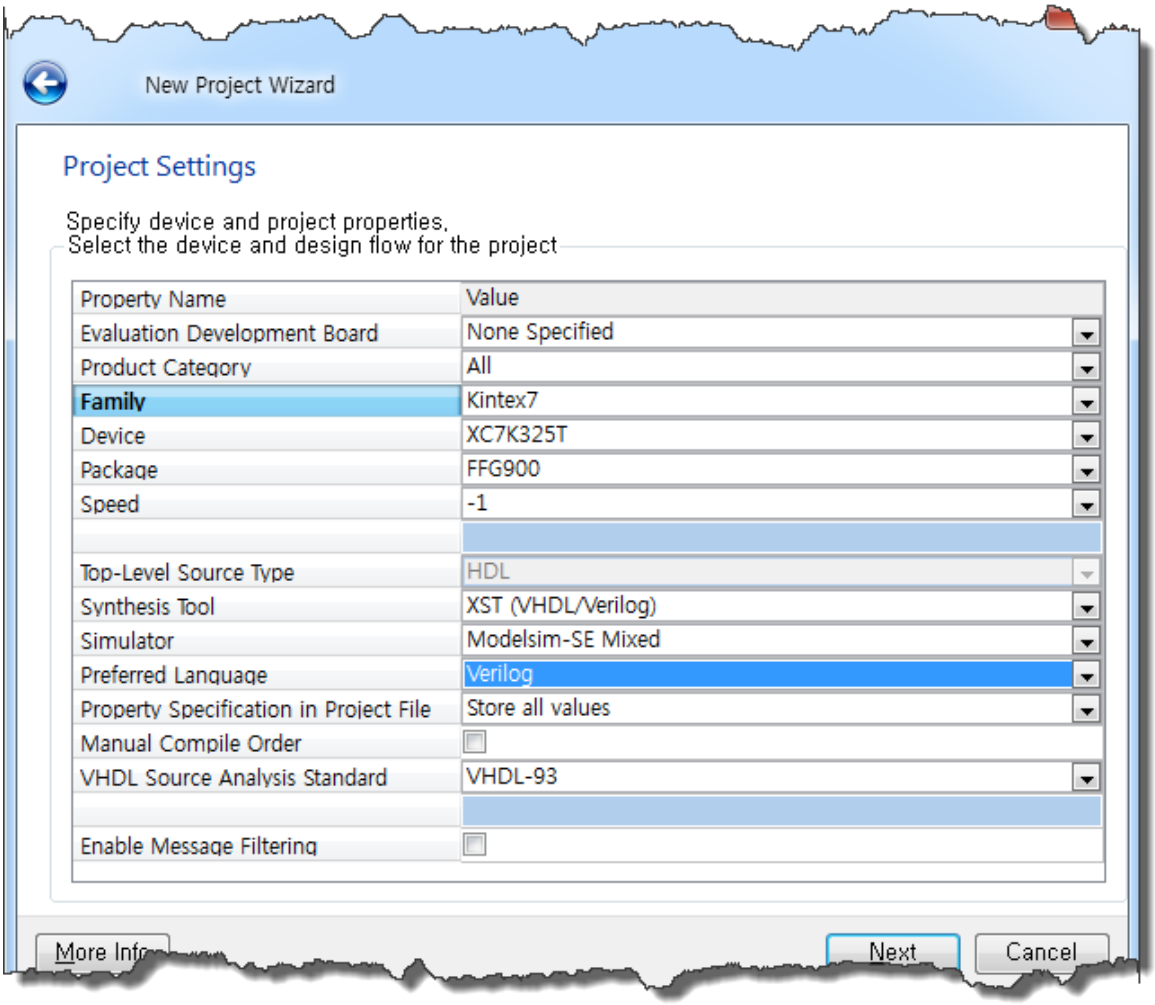


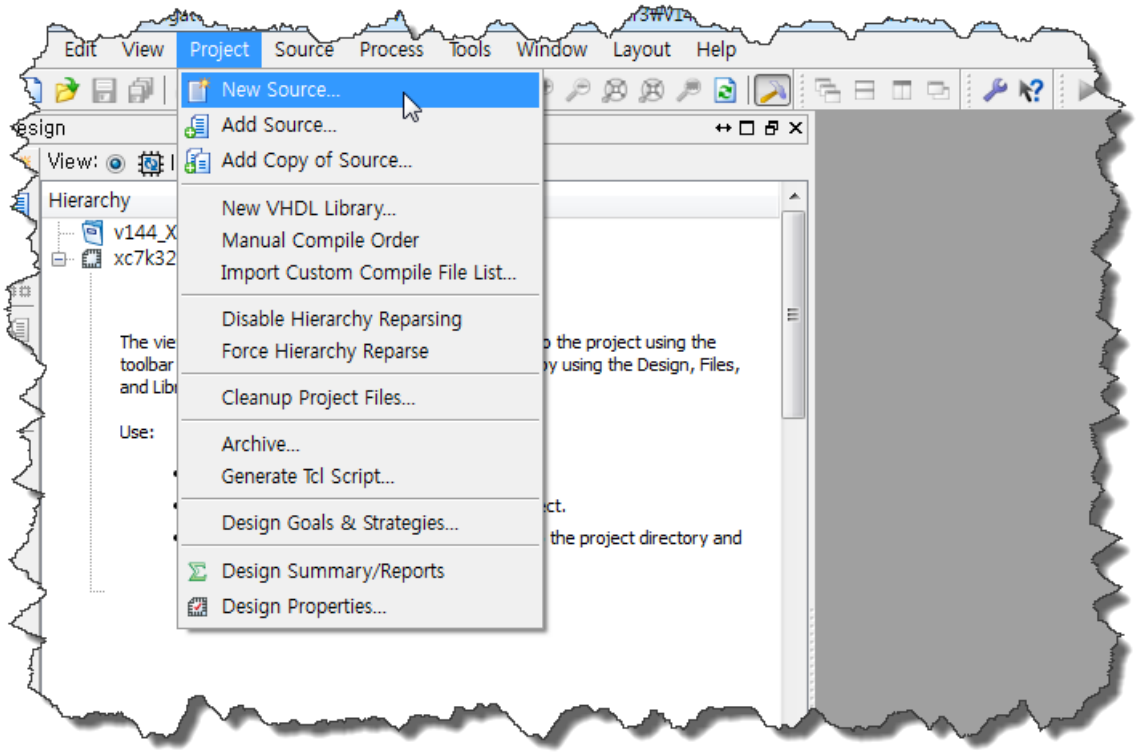
메모리 콘트롤러가 생성됩니다.

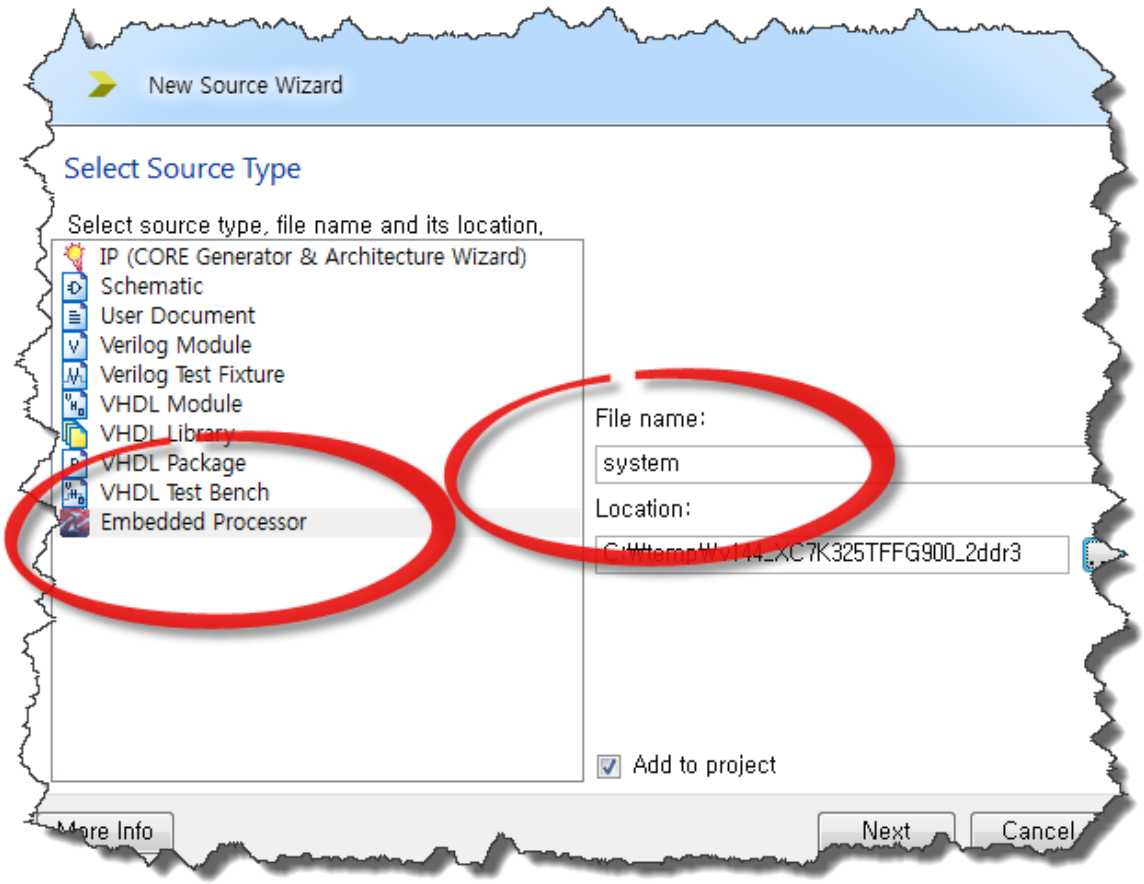


1.3 ISE

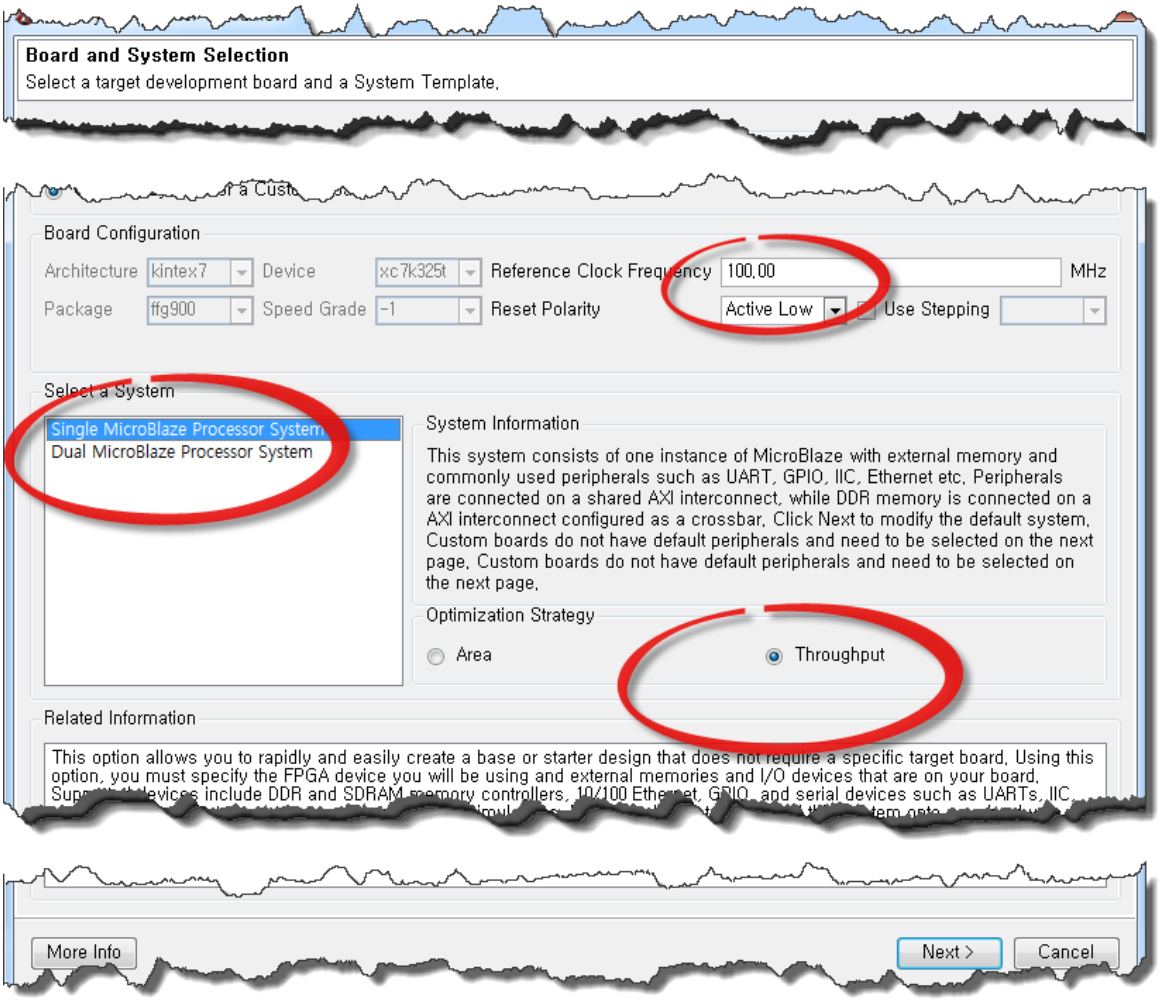

New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name:
v144_XC7K325TFFG900_2ddr3
Location:
C:₩temp₩v144_XC7K325TFFG900_2ddr3
Working Directory:
C:₩temp₩v144_XC7K325TFFG900_2ddr3
Description:
More Info
Next
Cancel


New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Kintex7
Device
XC7K325T
Package
FFG900
Speed
-1
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
Modelsim-SE Mixed
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
Next
Cancel

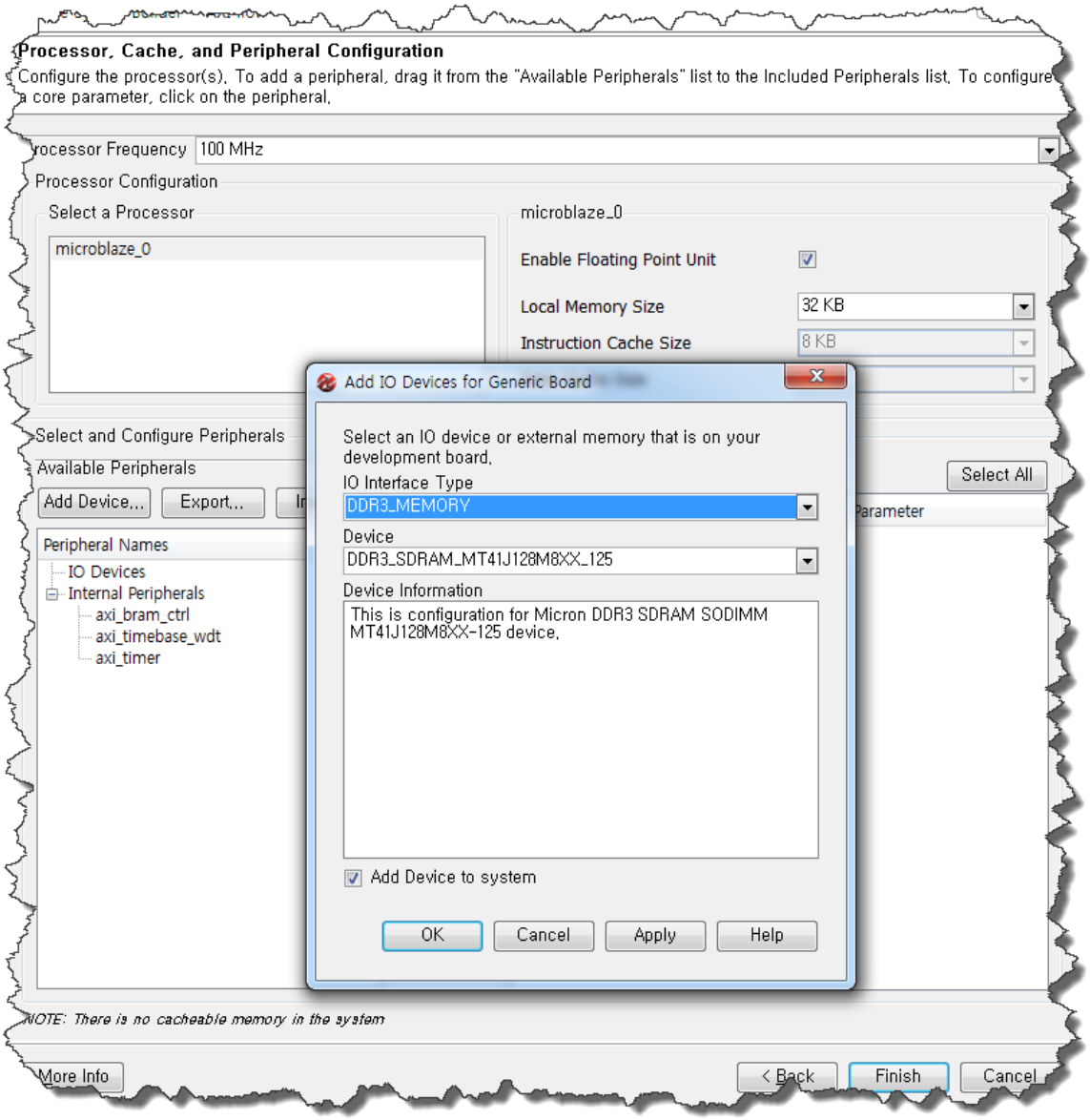

Edit
View
Project
Source
Process
Tools
Window
Layout
Help
New Source...
Add Source...
Add Copy of Source...
New VHDL Library...
Manual Compile Order
Import Custom Compile File List...
Disable Hierarchy Reparsing
Force Hierarchy Reparse
Cleanup Project Files...
Archive...
Generate Tcl Script...
Design Goals & Strategies...
Design Summary/Reports
Design Properties...
View:
Hierarchy
Use:

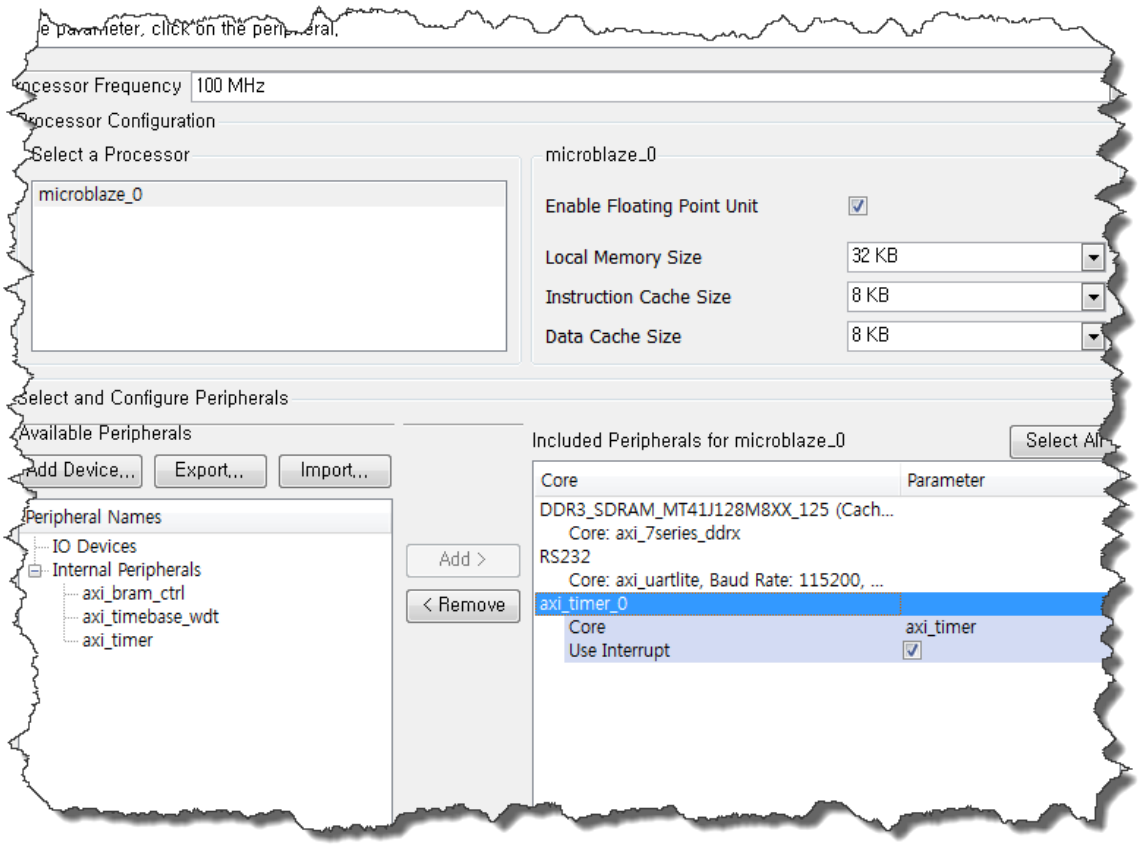


FPGA 외부에서 입력되는 주파수 값을 정하고 Reset 의 Polarity 도 정합니다.

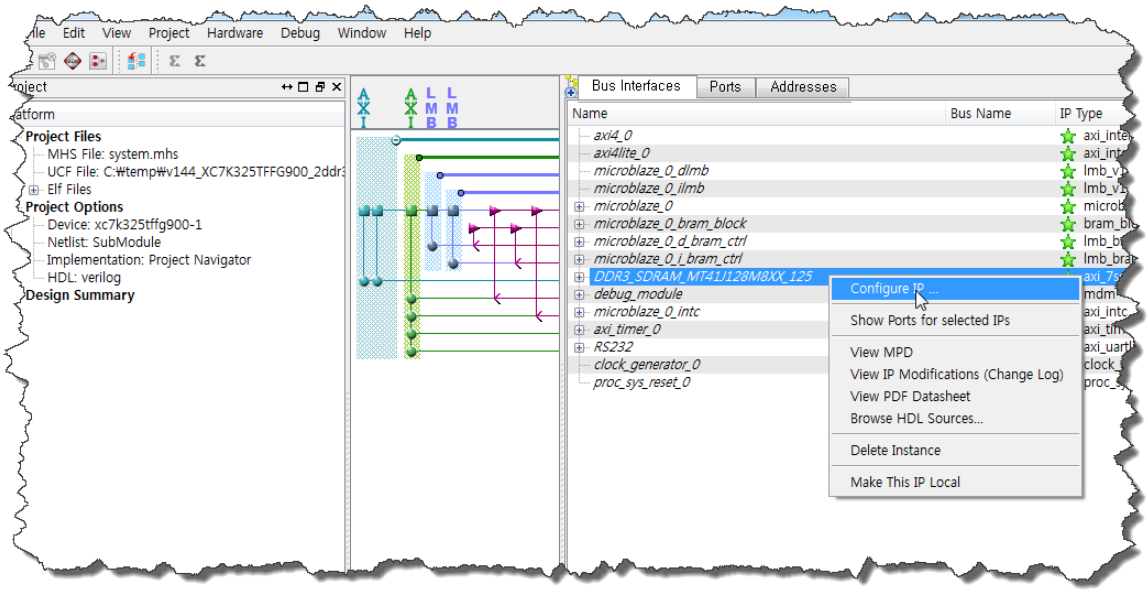


Add Device 에서 메모리 콘트롤러를 선택 하고 UART 나 Timer 등 기본적인 주변장치를 선택 합니다.

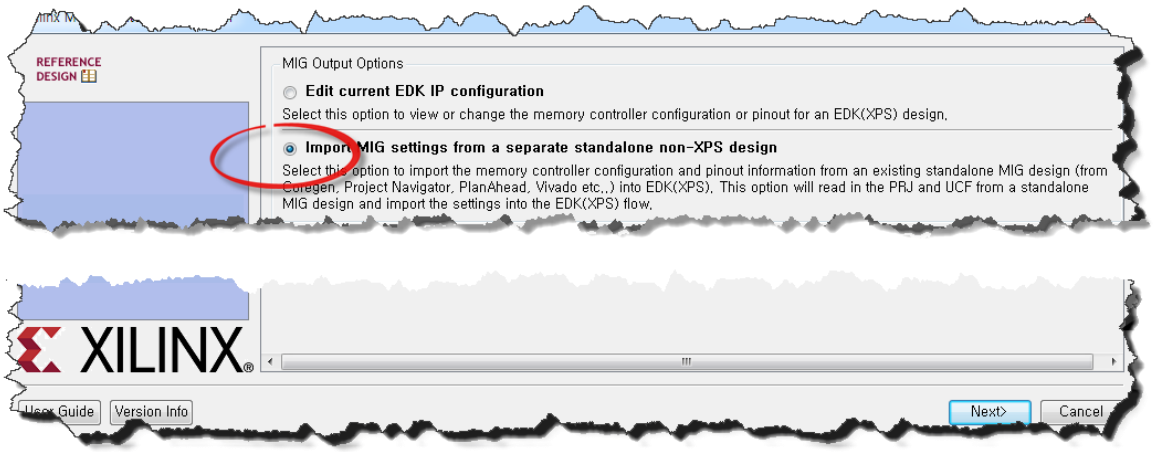

Processor, Cache, and Peripheral Configuration
Configure the processor(s). To add a peripheral, drag it from the "Available Peripherals" list to the Included Peripherals list. To configure a core parameter, click on the peripheral.
Processor Frequency
100 MHz
Processor Configuration
Select a Processor
microblaze_0
microblaze_0
Enable Floating Point Unit
Local Memory Size
32 KB
Instruction Cache Size
8 KB
Add IO Devices for Generic Board
Select an IO device or external memory that is on your development board.
IO Interface Type
DDR3_MEMORY
Device
DDR3_SDRAM_MT41J128M8XX_125
Device Information
This is configuration for Micron DDR3 SDRAM SODIMM MT41J128M8XX-125 device.
Add Device to system
OK
Cancel
Apply
Help
Select and Configure Peripherals
Available Peripherals
Add Device...
Export...
Select All
Parameter
Peripheral Names
IO Devices
Internal Peripherals
axi_bram_ctrl
axi_timebase_wdt
axi_timer
NOTE: There is no cacheable memory in the system
More Info
< Back
Finish
Cancel



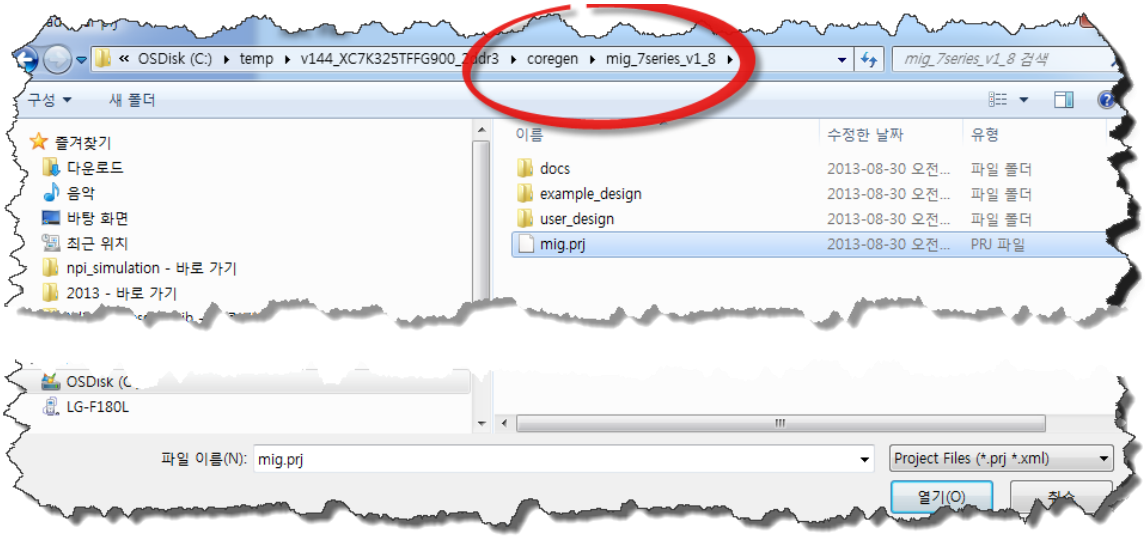
기본 셋팅이 되어 있는 메모리 콘트롤러를 MIG 에서 만들어진 콘트롤러로 바꾸려고 합니다.

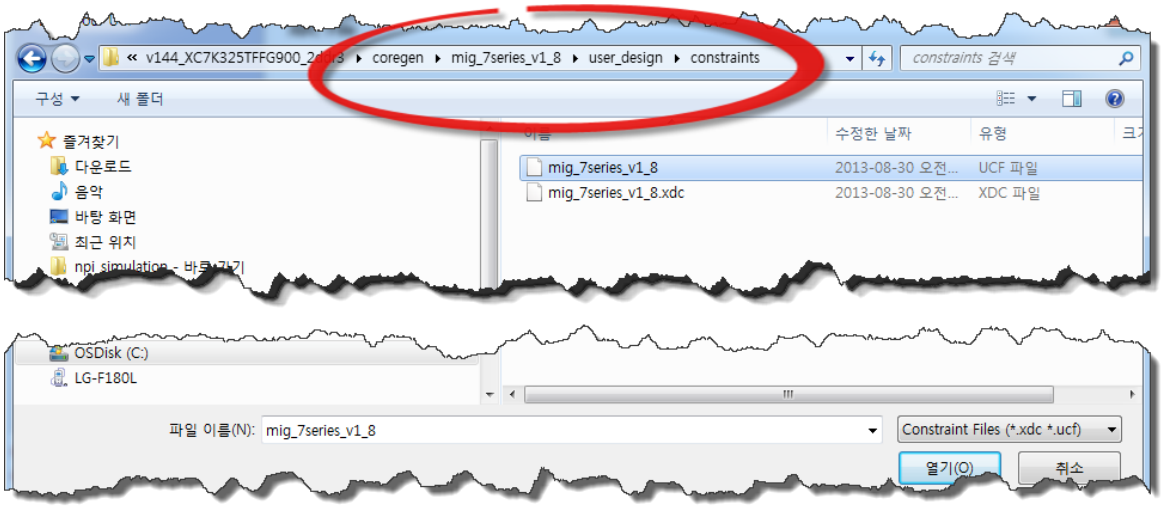


Coregen 에서 실행한 화면과 비슷한 화면이 나타나는데 이때 “Import...”를 선택 합니다.

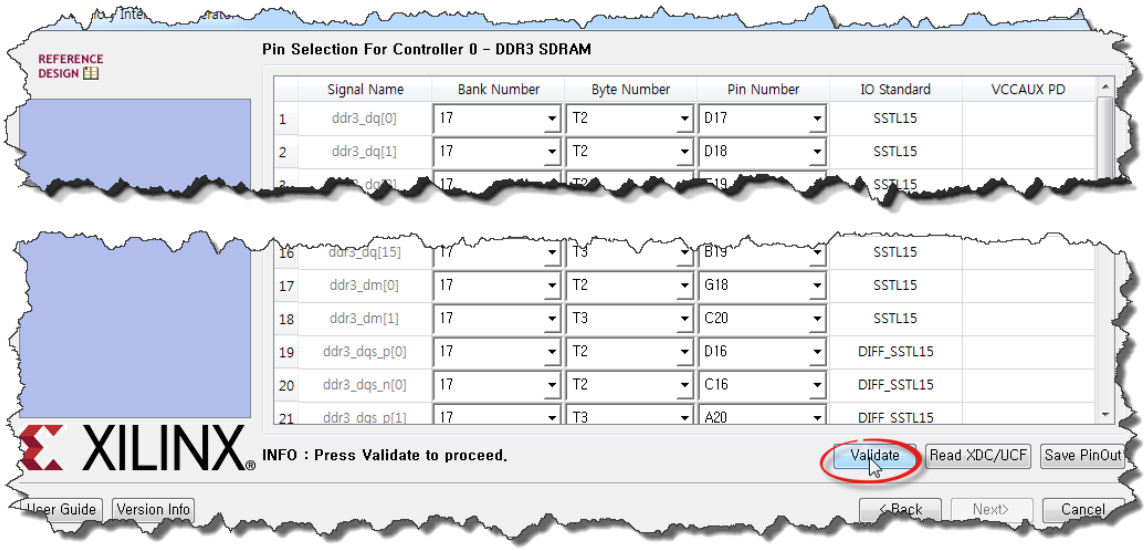


그러면 Project file 과 Ucf file 을 물어 보는데 Coregen 에서 만든 MIG 폴더에서 원하는 두개의 파일을 선택 합니다.

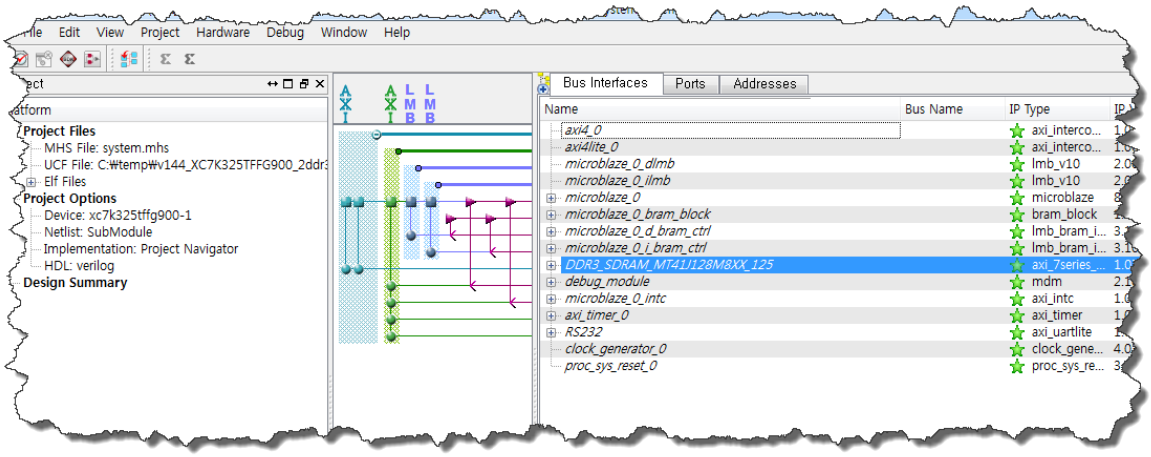




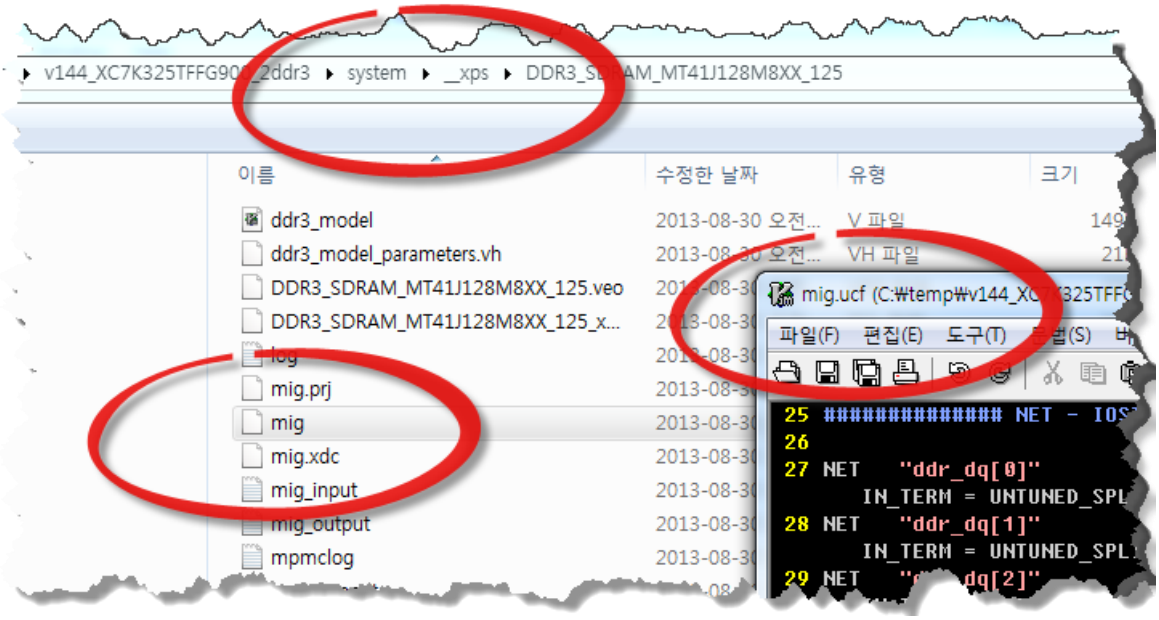
핀 정보가 문제 없는지 살펴봅니다.



필요한 경우 메모리 콘트롤러의 이름을 바꿀 수 있습니다.



이렇게 생성된 메모리 콘트롤러의 UCF 는 현재 EDK_Prj/__xps/DDR3.... 폴더에 MIG.UCF 로 저장 됩니다.



다음 리스트 수정된 MHS file 입니다.

```
1
2   # ##############################################################################
3   # Created by Base System Builder Wizard for Xilinx EDK 14.4 Build EDK_P.49d
4   # Fri Aug 30 10:55:24 2013
5   # Target Board:  Custom
6   # Family:    kintex7
7   # Device:    xc7k325t
8   # Package:   ffg900
9   # Speed Grade:  -1
10  # ##############################################################################
11   PARAMETER VERSION = 2.1.0
12
13
14   PORT RS232_Uart_1_sout = RS232_Uart_1_sout, DIR = O
15   PORT RS232_Uart_1_sin = RS232_Uart_1_sin, DIR = I
16   PORT RESET = RESET, DIR = I, SIGIS = RST, RST_POLARITY = 0
17   PORT DDR3_SDRAM_we_n = DDR3_SDRAM_we_n, DIR = O
18   PORT DDR3_SDRAM_ras_n = DDR3_SDRAM_ras_n, DIR = O
19   PORT DDR3_SDRAM_odt = DDR3_SDRAM_odt, DIR = O
20   PORT DDR3_SDRAM_dqs_n = DDR3_SDRAM_dqs_n, DIR = IO, VEC = [1:0]
21   PORT DDR3_SDRAM_dqs = DDR3_SDRAM_dqs, DIR = IO, VEC = [1:0]
22   PORT DDR3_SDRAM_dq = DDR3_SDRAM_dq, DIR = IO, VEC = [15:0]
23   PORT DDR3_SDRAM_dm = DDR3_SDRAM_dm, DIR = O, VEC = [1:0]
24   PORT DDR3_SDRAM_ddr3_rst = DDR3_SDRAM_ddr3_rst, DIR = O
25   PORT DDR3_SDRAM_cs_n = DDR3_SDRAM_cs_n, DIR = O
26   PORT DDR3_SDRAM_clk_n = DDR3_SDRAM_clk_n, DIR = O, SIGIS = CLK
27   PORT DDR3_SDRAM_clk = DDR3_SDRAM_clk, DIR = O, SIGIS = CLK
28   PORT DDR3_SDRAM_cke = DDR3_SDRAM_cke, DIR = O
29   PORT DDR3_SDRAM_cas_n = DDR3_SDRAM_cas_n, DIR = O
30   PORT DDR3_SDRAM_ba = DDR3_SDRAM_ba, DIR = O, VEC = [2:0]
31   PORT DDR3_SDRAM_addr = DDR3_SDRAM_addr, DIR = O, VEC = [15:0]
32   PORT CLK_P = CLK, DIR = I, DIFFERENTIAL_POLARITY = P, SIGIS = CLK, CLK_FREQ =
100000000
33   PORT CLK_N = CLK, DIR = I, DIFFERENTIAL_POLARITY = N, SIGIS = CLK, CLK_FREQ =
100000000
34

//////////////////////////////////////////////////////
```

```
BEGIN axi_7series_ddrx
 PARAMETER INSTANCE = DDR3_SDRAM_MT41J128M8XX_125
 PARAMETER HW_VER = 1.07.a
 PARAMETER C_MEM_PARTNO = k4b4g1646b
 PARAMETER C_INTERCONNECT_S_AXI_AR_REGISTER = 8
 PARAMETER C_INTERCONNECT_S_AXI_AW_REGISTER = 8
 PARAMETER C_INTERCONNECT_S_AXI_R_REGISTER = 8
 PARAMETER C_INTERCONNECT_S_AXI_W_REGISTER = 8
 PARAMETER C_INTERCONNECT_S_AXI_B_REGISTER = 8
 PARAMETER C_DM_WIDTH = 2
 PARAMETER C_DQS_WIDTH = 2
 PARAMETER C_DQ_WIDTH = 16
 PARAMETER C_ROW_WIDTH = 16
 PARAMETER C_INTERCONNECT_S_AXI_MASTERS = microblaze_0.M_AXI_DC &
microblaze_0.M_AXI_IC
 PARAMETER C_S_AXI_DATA_WIDTH = 128
 PARAMETER C_S_AXI_BASEADDR = 0xb0000000
 PARAMETER C_S_AXI_HIGHADDR = 0xbfffffff
 PARAMETER C_BANK_TYPE = HR_IO
 PARAMETER C_RTT_NOM = 60
 PARAMETER C_TCK = 2500
 PARAMETER C_PLLE2_EXT_LOC = X0Y4
 PARAMETER C_CLKOUT0_PHASE = 337.5
 BUS_INTERFACE S_AXI = axi4_0
 PORT clk = clk_100_0000MHzPLLE0
 PORT ddr_we_n = DDR3_SDRAM_we_n
 PORT ddr_ras_n = DDR3_SDRAM_ras_n
 PORT ddr_odt = DDR3_SDRAM_odt
 PORT ddr_dqs_n = DDR3_SDRAM_dqs_n
 PORT ddr_dqs_p = DDR3_SDRAM_dqs
 PORT ddr_dq = DDR3_SDRAM_dq
 PORT ddr_dm = DDR3_SDRAM_dm
 PORT ddr_reset_n = DDR3_SDRAM_ddr3_rst
 PORT ddr_cs_n = DDR3_SDRAM_cs_n
 PORT ddr_ck_n = DDR3_SDRAM_clk_n
 PORT ddr_ck_p = DDR3_SDRAM_clk
 PORT ddr_cke = DDR3_SDRAM_cke
 PORT ddr_cas_n = DDR3_SDRAM_cas_n
 PORT ddr_ba = DDR3_SDRAM_ba
 PORT ddr_addr = DDR3_SDRAM_addr
 PORT sync_pulse = clk_25_0000MHz9.84375PLLE0_nobuf
 PORT mem_refclk = clk_400_0000MHzPLLE0_nobuf
 PORT freq_refclk = clk_400_0000MHz337.5PLLE0_nobuf
 PORT clk_ref = clk_200_0000MHzPLLE0
 PORT pll_lock = proc_sys_reset_0_Dcm_locked
END
```